MULTIMEDIA UNIVERSITY ™

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 3, 2015/2016

EEE1036 – DIGITAL LOGIC DESIGN

(All sections / Groups)

30 MAY 2016
9.00 a.m - 11.00 a.m
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This question paper consists of 5 pages with 4 questions only.

2. Answer all **FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please write all your answers in the Answer Booklet provided.

Question 1 (25 marks)

(a) Explain the difference between digital and analog systems. Give an example for each of digital and analog systems.

[4 marks]

(b) Describe the limitation of digital systems.

[2 marks]

(c) Name **TWO (2)** main families of logic devices. Differentiate between them by stating **THREE** characteristics for each family.

[8 marks]

(d) Convert the given numbers in **Table 1** to other specified bases listed accordingly.

[8 marks]

Table 1

Binary	Octal	Decimal	Hexadecimal
	555.64		16D.D
100110111.110		311.75	

(e) Perform BCD addition between 69 and 28.

[3 marks]

Continued ...

Question 2 (25 marks)

(a) Simplify the expression below using the DeMorgan's Theorems.

$$\overline{\overline{(A+B)}\,\overline{(C+D)}\,\overline{(E+F)}\,\overline{(G+H)}}$$

[5 marks]

(b) Convert and simplify the expression below to sum-of-product (SOP) form

$$A+B[(B+\overline{C})D+AC]$$

[5 marks]

(c) Show the steps to modify your results from Q2 (b) to use only NOR gates. Following that, draw its logic circuit.

[5 marks]

(d) Design a logic system that detects prime numbers between 0 and 9. Your design employs a BCD code that consists of 4 digits, which means that you will treat the output for the remaining decimal equivalent numbers i.e. 10 to 15 as 'don't care'. Draw the truth table for the system and use Karnaugh Map to find the simplified SOP logic expression.

[5 marks]

(e) **Table 2** shows the Prime Implicant table that has been derived using Quine-Mcluskey method for a logic system. Find the minimum SOP of the system.

Table 2

	0	2	5	6	7	8	10	12	13	14	15
PI_1: B'D'	X	X				X	X				
PI_2: CD'		X		X			X			X	
PI_3: BD			X		X				X		X
PI_4: BC				X	X					X	X
PI_5: AD'						X	X	X		X	
PI_6: AB								X	X	X	X

[5 marks]

Continued ...

Question 3 (25 marks)

(a) Briefly describe Synchronous and Asynchronous Sequential Circuits.

[4 marks]

(b) The input signals shown in **Figure 3(b)** are applied to the gated D-latch when initially in its zero state. Redraw the input signals and sketch the corresponding output signals, Q based on the given input D-latch and clock. Assume all timing constraints are satisfied.

[5 marks]

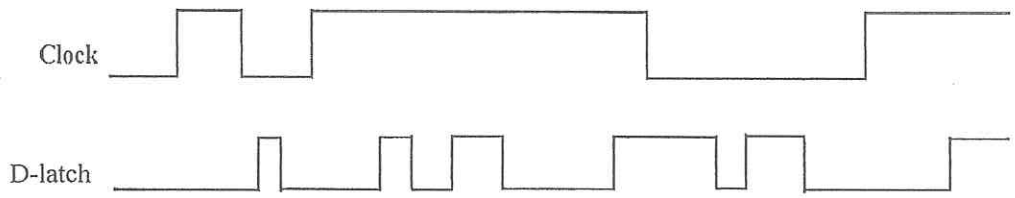

Figure 3(b)

(c) A synchronous counter goes through the counting sequence 0, 1, 2, 6, and repeats.

(i) Design the counter using positive-edge triggered *JK* flip-flops. The design should include required flip flops truth table, transition table, and Karnaugh map with minimum number of logic gates. Clear working steps with labels must be shown.

[8 marks]

(ii) Repeat the design process using negative–edge triggered *T* flip flops. Clear working steps with labels must be shown.

[8 marks]

Continued ...

Question 4 (25 marks)

(a) Draw a schematic symbol of a 1-bit full adder, showing its inputs and outputs. [3 marks]

(b) Draw a schematic diagram of a 3-bit ripple-carry adder, showing how it is made of 1-bit full adders. [3 marks]

(c) With the aid of a schematic diagram (please draw), suggest a way to connect 8 sensors with binary output to one input port, such that the sensors' state can be read via the input port. [4 marks]

(d) With the aid of a schematic diagram (please draw), suggest a way to connect four 64 kbytes (16-bit address) memory modules to an 18-bit address bus, such that they collectively provide 4×64 kbytes of memory space.

Draw the address buses as bundles and label them with the range of address bits they represent, for example shown in **Figure 4 (d)**. [5 marks]

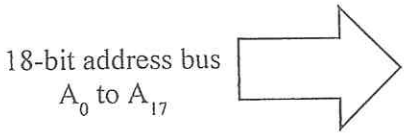

Figure 4 (d)

(e) Implement switching function $f(x, y, z) = \sum m(0,2,4,5,6,7)$ using each of the following:

(i) 3-to-8 decoder with active high outputs. [5 marks]
(ii) 4-to-1 multiplexer. [5 marks]

Please draw the schematic diagrams. For the multiplexer implementation, show the truth table.

End of Paper